

CMOS TESTING

Introduction:-

- After the chip is fabricated it is tested for manufacturing defects. The chip designer must verify (or) validate the design to ensure the ckt performance. Verification (or) validation is a different process than testing.
- verification is related to formal proof of correctness. while validation is a technique that increases confidence in correctness.
" If you don't test it, it won't work! (Guaranteed)"

Need for Testing:

- During fabrication process several types of defects may exists such as catastrophic, crystalline.
- a) catastrophic defect is due to contamination, resulting in destruction of all the transistors on the chip
- b) crystalline defect is because of destruction of a single transistor on the chip.

→ It is necessary to test the chip from the flaws. Hence it mandatory to check the chip regarding its performance and functionality.

Identifying the faulty chips is a complex job & also time consuming. The faulty chip creates huge difficulty in system debugging. It also increases the debugging cost. Therefore the design for Testability (DFT) is necessary.

→ The testing is performed in two steps:

- 1) Functionality Test
- 2) Manufacturing Test

Functionality Test:

→ Functionality Tests are the first tests that are performed during design process. Functionality tests ensures that all the gates in the chip acting in concert and achieve a desired function to verify the functionality of the circuit.

→ In most systems functionality tests involves proving the circuit is functionally equivalent to some specification. Functional equivalence involves running a simulator at some level with all inputs applied and outputs are equivalent. The functional equivalence can be carried out at various levels of the design hierarchy.

→ There is no good theory to ensure good functional tests. But it is best advice that to simulate the chip or system as closely as possible as it will be used in real world. One approach is to move simulation hierarchy after verification of modules at lower level.

Manufacturing Tests:

→ Functionality test verify the function of chip as a whole, whereas manufacturing tests used to verify that every gate operates as expected. The manufacturing defects occurs during chip

fabrication or during accelerated life testing.

→ commonly observed defects & their results are mentioned as under.

S.No	Defects	Result.
1)	layer-to-layer shorts (metal to metal)	nodes shorted to power (or) GND
2)	Discontinuous wires (metal) thins when crossing vertical topology jumps	 nodes shorted to each other
3)	Thin-oxide shorts to substrate (or) well	Inputs floating/ outputs disconnected

Manufacturing test verify that each gate and register is operational. These tests are carried out at wafer level, to reject bad die.

→ The I/O integrity is tested by following tests.

1) I/O- level test (check of noise margin for TTL, ECL and CMOS)

2) Speed test

3) IDD test (checks the leakage of circuit).

→ Water test is carried out at high speed or low speed (1 MHz) due to possibility of power & ground bounce effects.

Comparison of Functionality Test & Manufacturing Test:

S.No.	Functionality Test	Manufacturing Test
1.	The functionality test verifies that the chip performs its intended function. i.e., these tests ensure that all the gates in the chip performs desired function.	The manufacturing test verifies that every gate and register in the chip functions correctly.
2.	Functionality tests usually performs early in the design cycle to verify functionality of the circuit	2. The manufacturing tests are used after the chip is manufactured to verify that the silicon is intact.

3. This test performs test of instruction or sequence to check that registers of instructions can store a_1 and a_0 .
4. Functionality test generation Manufacturing test assumes that the address generation assumes multiplexers, gates and that circuit/chip registers operate correctly functions correctly on.

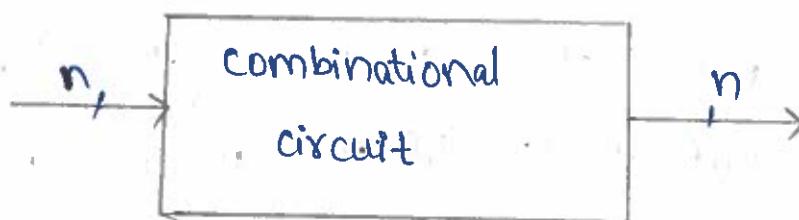
Test principles:-

→ Different test principles are incorporated in design and manufacturing of VLSI circuits. For testing a circuit exhaustively large number of test vectors are needed, which is not feasible even at very high speed. Fortunately the no. of non-functional nodes on a chip is smaller than the no. of states. A manufacturing test engineer must device test vectors for clearly detecting any defective node without requiring so many patterns.

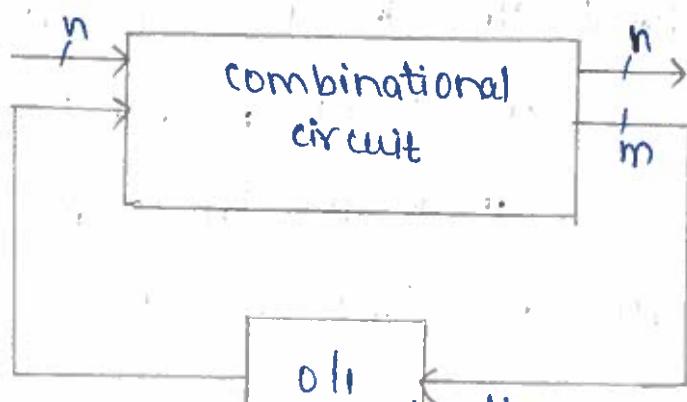
→ The below figure illustrates testing of combinational circuit with 2^n test vector (n -inputs). The combinational circuit is converted to sequential circuit by adding m -storage registers

→ The state of sequential circuit is determined by inputs and previous input condition. Minimum test vectors $&^{(m+n)}$ are required to be applied to test this circuit.

Testing of combinational circuit.



n -inputs required



Registers

Fault models:

→ A model for how fault occurs and their impact on circuits is called a fault model. A fault model for every circuit is proposed before actual testing.

Two proper fault models are:

1) stuck-at faults

2) stuck-open or stuck-short faults.

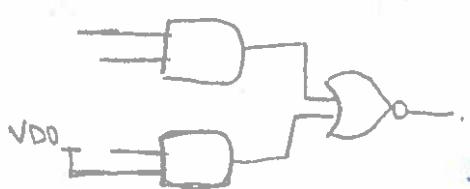
Stuck-at fault model is most popular and simpler model. A stuck-open or stuck-short model is more close to the real behaviour of circuit but it is difficult to incorporate.

Stuck-at faults:

Stuck-at fault model assigns a fixed value (0 or 1) to signal line in the circuit, which is an input or output of a gate/flip-flop. Popular forms of stuck-at fault are single stuck-at faults two fault per line (stuck-at-1, stuck-at-0).

The properties that fault model must possess are as under-

- 1) The model must corresponds to real faults.
 - 2) The model must have adequate granularity.
 - 3) The model must be accountable.
 - 4) The model must be automated.
- The stuck-at fault model even though corresponds to real faults but it does not represent all possible faults.
- Granularity means resolution at which a model represents faults. A fault model with fine granularity is more useful than a model with coarse granularity.
- The fault models can be deduced by using basic circuits such as AND, OR, Inverter and tri-state buffer.
- The below fig. Shows how S-A-0 or S-A-1-fault occurs.



stuck - At - 0. (S-A-0 fault)

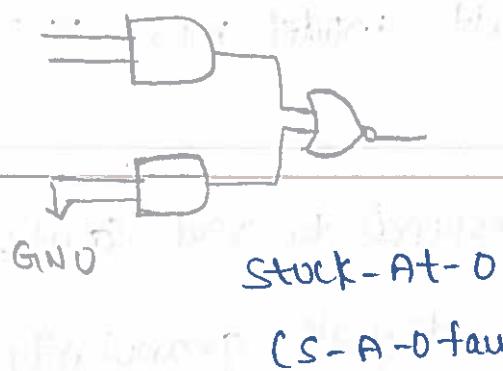


Fig: CMOS stuck-at-faults.

→ Stuck-at-faults mostly occur due to shorting of gate oxide (NMOS gate to GND or PMOS gate to VDD) or metal-to-metal shorts

Stuck-open and stuck-short faults:

→ Stuck-open and stuck-short faults are usually referred as transistor faults. physical faults which occurs at manufacturing level are called as defects. The electrical or logic-level faults by physical defects are referred as defect oriented faults such as open links, improper semiconductor doping, bridging faults etc...

→ consider a MOS transistor to be modelled as ideal switch. The defect may be switch being permanently in open state or short state.

This fault model involves just one transistor as stuck-open or stuck-short. The below fig shows a CMOS NOR logic circuit to illustrate this model.

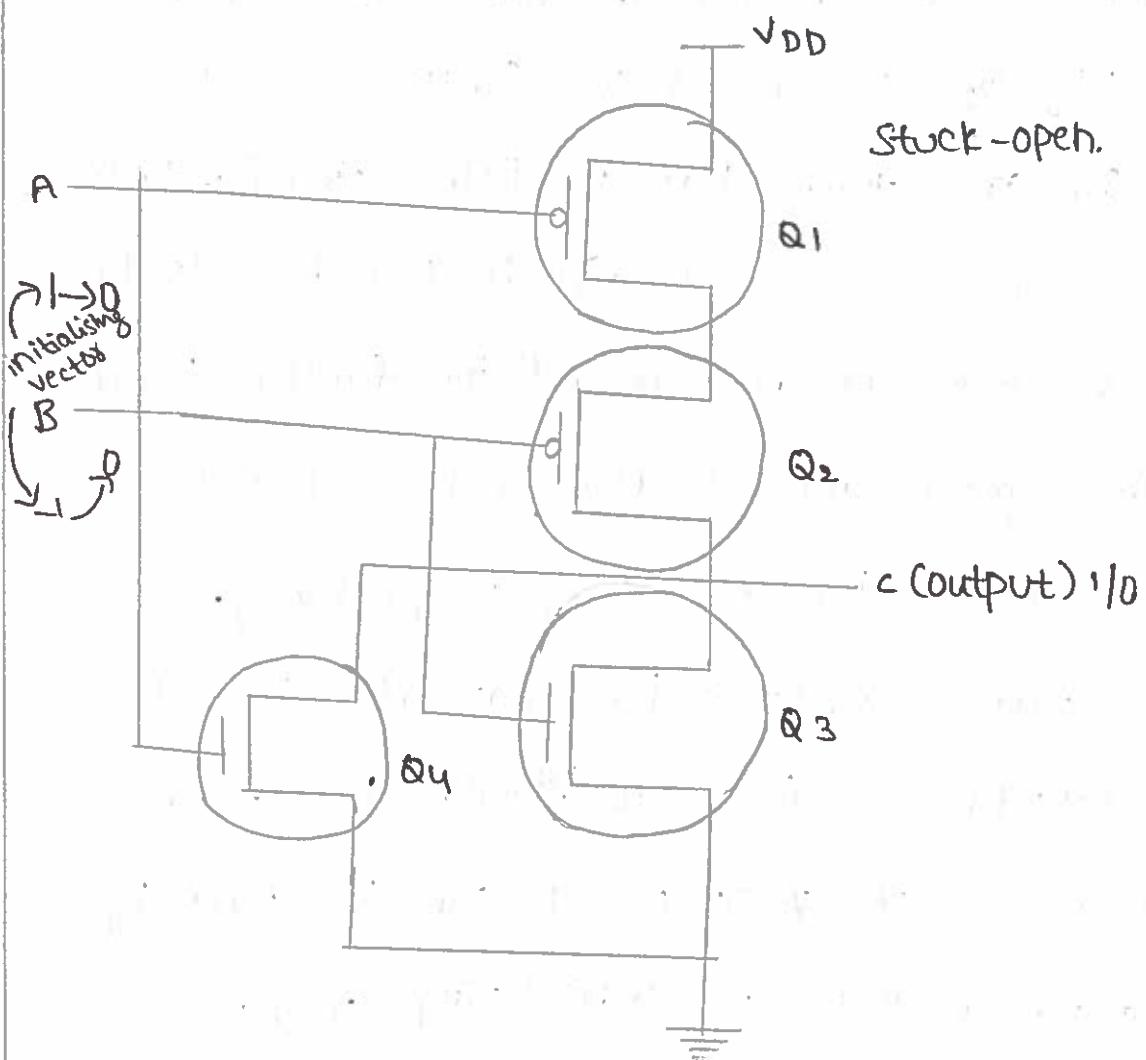


fig: CMOS NOR logic

Stuck-open fault:

→ Q₁ and Q₂ are PMOS transistors and Q₃ and Q₄ are NMOS transistors. When gate inputs A and B are '0', transistors Q₁, Q₂ are shorted

and Q_3, Q_4 are open. Therefore when $A=B=0$, output c is connected to V_{DD} . similarly when $A=B=1$ output c is connected to ground i.e., 0.

→ Suppose fault Q_1 stuck-open. If $A=B=0$ then Q_1 and Q_2 are shorted in fault free circuit but only Q_2 is shorted in faulty circuit Q_3 and Q_4 are given open in both circuit. Hence output c is '1' in good circuit but is floating (neither top V_{DD} nor ground) in faulty circuit.

The good and faulty states of output c are denoted by z and $\frac{1}{z}$ respectively.

→ The output node c has parasitic capacitance. For detecting a fault, it should be ensured that value of z is 0. It can be done by preceding $A=B=0$ as initializing vector to $A=1, B=0$. This sets output node c to 0 in faulty circuit by discharging node capacitance to ground potential.

→ To complete the test another input from 10 to 00 is applied. It produces an output 0 → 1

in. good circuit and $0 \rightarrow 0$ in faulty circuit.

Observability:

Observability is a degree to which it can be observed that node at output operates correctly. Observability is useful, when a test engineer has to measure the output of a gate/chip within a larger circuit. To check its correct operation. Higher observability indicates + less no. of cycles required to measure output node value. Circuit having poor observability includes sequential circuits with long feedback loops.

Controllability:

- Controllability is the ability of an internal circuit within a chip the ease setting the node to logic 1 or 0 state.
- Controllability is important while accessing the degree of difficulty of testing a particular signal in a circuit
-

→ A node with little controllability may take hundreds of cycles to get it to the right state.

Fault coverage:

→ Ideally testing involve detecting all possible faults in a device under Test (DUT). The extent of testing decides the percentage of faults that can be detected. Detection of all possible faults in a DUT corresponds to 100% test coverage.

→ Fault coverage is defined as the percentage of the fault that be detected by the applied test vector. Fault coverage gives a measure of goodness of a test program. High fault coverage is desirable during manufacturing test. Design for Testability (DFT) is used to improve the fault coverage.

Steps to find Fault coverage:

- 1) Each circuit node held to logic '0' (S-A-0) one by one.
- 2) The output of chip is compared with 'good machine'.
- 3) If the output is deviated, the machine is marked as 'faulty machine'.
- 4) Repeat the above steps by setting the circuit node to logic '1' (S-A-1).
- 5) Fault coverage in percentage is given as:

1. Fault coverage = $\frac{\text{Number of faults detected}}{\text{Total nodes in the circuit}}$

Total number of cycles to be simulated = $K \times N$

where, K is number of nodes in the circuit

N is length of test sequence.

Fault simulation:

Fault simulation is defined as the process of measuring the quality of test. Fault

simulation is performed using gate level model and functional level model.

Fault simulation serves following functions:

- 1) confirms detection of fault.
- 2) computes fault coverage
- 3) Diagnostics of circuit.
- 4) Identifies areas of circuit where fault coverage is inadequate.

Design strategies for Test:-

- 1) Design for Testability (DFT):-
 - Design for Testability shows the fault model to test the chip in manufacturing process.
 - The aspect of testability is based on two key concepts. i.e., controllability and observability.
- The inclusion of these concepts means the provision of some means for setting and resetting key nodes in the system, and then observing the response at key points in the system. Design for Testability is

then just a set of design rules or guidelines which, if obeyed will facilitate test. Any failure occurring during testing is due to either poorly controlled fabrication process or because of design defect.

→ Design for Testability. covers three important approaches.

- 1) Ad-hoc testing
- 2) Scan base approaches
- 3) Self-test & built in testing.

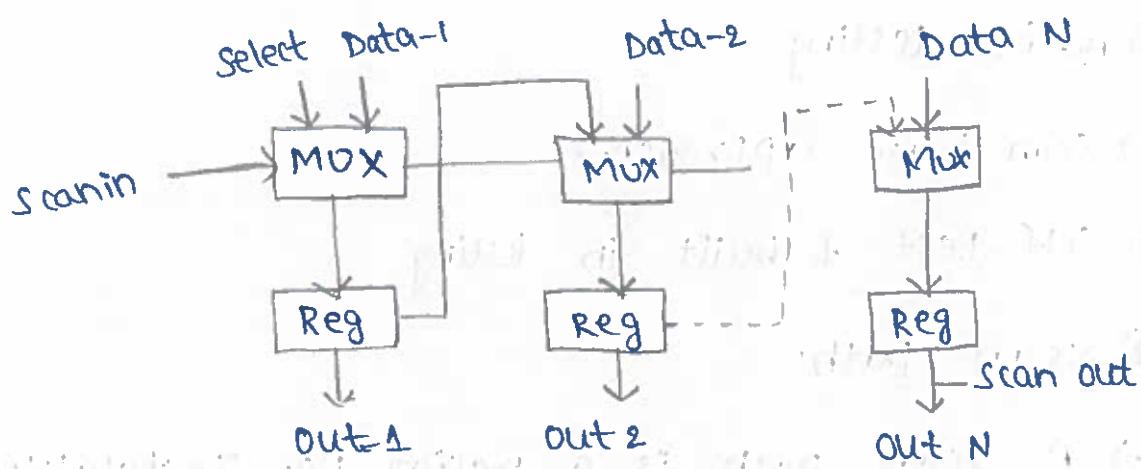
2) Scan path:

→ A scan path is a Design for Testability (DFT) technique which involves specialized flip-flop or latch allowing data to be scanned in for control and then out for observation and then activated in scan mode for test purposes.

→ A scan path consists → is tested by shifting a special pattern through the scan path

before the stuck at faults begins. The test pattern consists of 1s and 0s that test the ability of the scan path to shift all possible transitions.

→ A scan path consists of placing a multiplexer just at the head of each flip-flop as shown in below fig.



→ One input of Mux (2:1) is driven by operational data while other is driven by output of other flip-flop. The left most Mux is fed with the serial input (scan in) and output of last flip-flop is connected to primary output pin (scan out).

→ The data is serially shifted into scan

path when scan enable is high. The below fig shows waveforms for scan shift operation for positive clock edge controlled composed of four scan flip-flop.

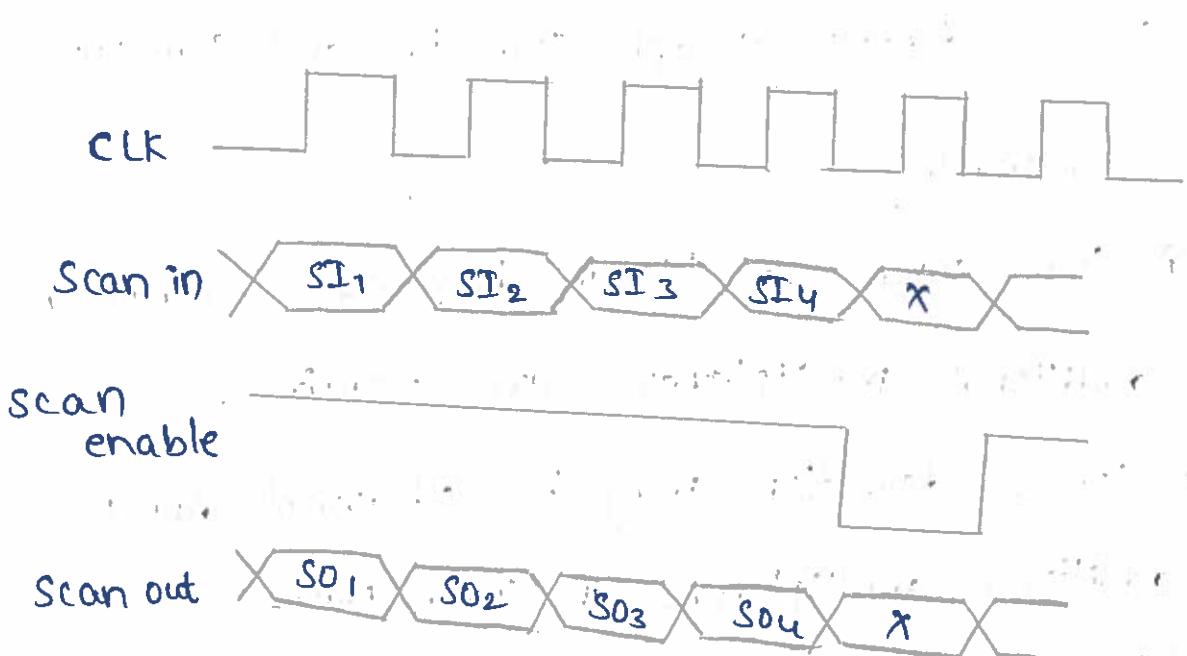


fig: Scan shift operation.

→ The scan shift operation simplifies the task of creating stimuli for sequential circuits. The scan operation also reduces the time of testing as multiple scan paths can run in parallel with same cost.

Advantages of scan path:

- 1) Test vector can be generated by automatic

test pattern generator

- 2) During design phase problems like observability and controllability need not to be considered.
- 3) NO need of complex test vector generator for all inputs except scan in and scan out.

Disadvantages:

- 1) Scan path results in hardware overhead as additional multiplexers are required.
- 2) Speed degradation may be observed due to additional multiplexers in signal path.
- 3) Full scan and Partial scan:
 - Sequential Automatic Test pattern Generator (ATPG) is used for partial scan and combinational ATPG is used for full scan.
 - Full scan provides total controllability and observability. Also full scan provides high fault coverage for structural defects. Full scan testing is carried out in two phases

phase-1- It tests the scan register by a shift test

phase-2: single stuck-at faults in combinational logic.

→ A full scan schematic is shown in below fig.

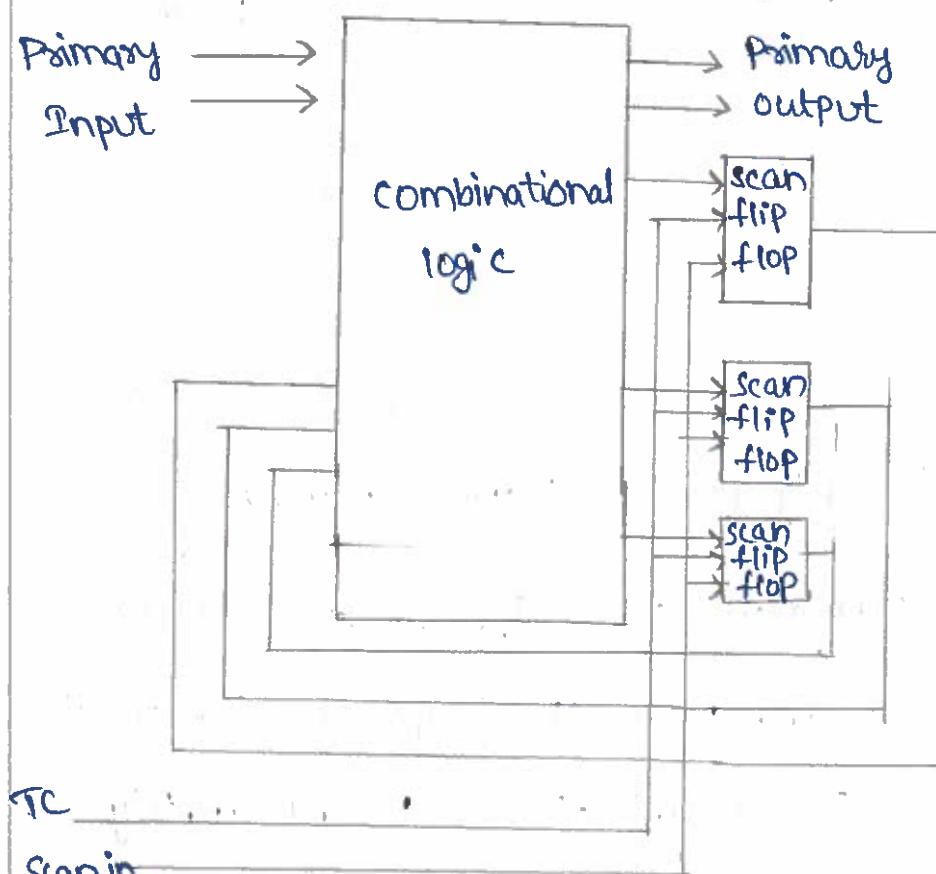


Fig: Full scan Schematic.

→ The test generation time is very small for full scan.

Partial scan:

In partial scan mode all the flip-flops are not into a scan path. The below fig. shows schematic of partial scan.

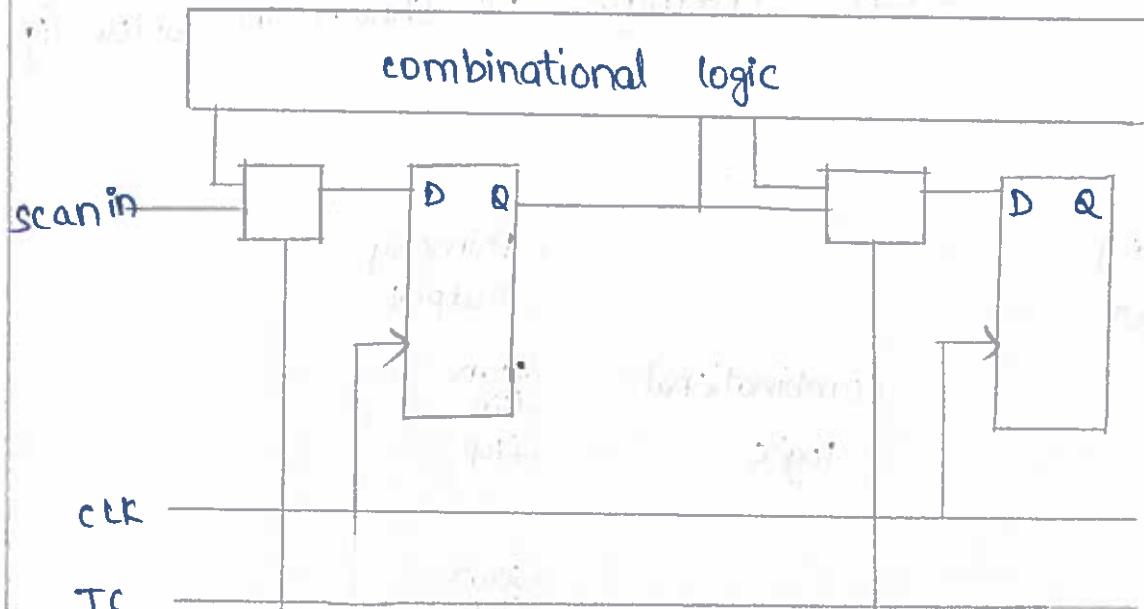


Fig: Partial scan schematic

→ The gate overhead is significantly lower for partial scan. Also it improves the fault coverage and fault efficiency to adequately high levels.

JTAG:

JTAG is IEEE 1149.1 standard for boundary scan. JTAG is meant for verifying

whether the circuit has been mounted a circuit board correctly. JTAG standard specifies method to test device functionality and inter-connections through test access port (TAP) and boundary scan.

- JTAG has the capability to transform any multiple complex printed circuit board problem into a well structured problem.
- JTAG method is employed for testing and quality assurance and also for debugging.
- JTAG also has a mode called Built-in-self-Test (BIST). BIST mode is used to limit the no. of vectors that need to be clocked through the scan path. A device in BIST mode generates pseudo random test-vectors as stimuli compares internal outputs against expected results and indicates success or failures.
- Use of JTAG to test internal outputs failures

JTAG TO test internal circuitry is shown in below fig.

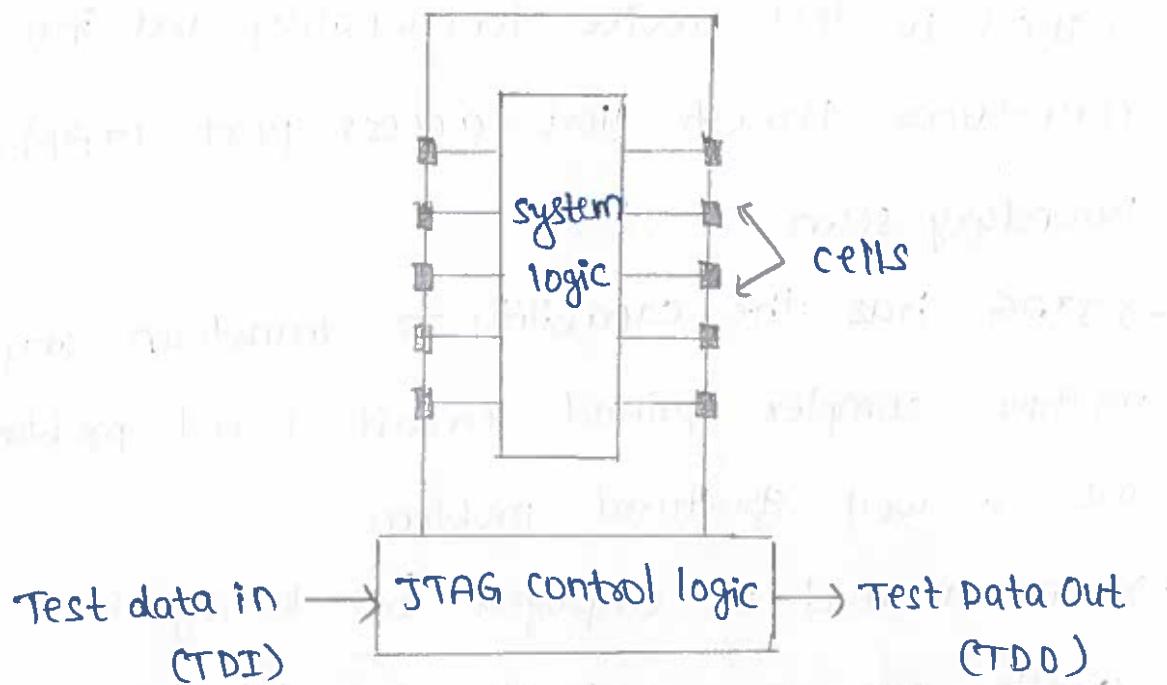
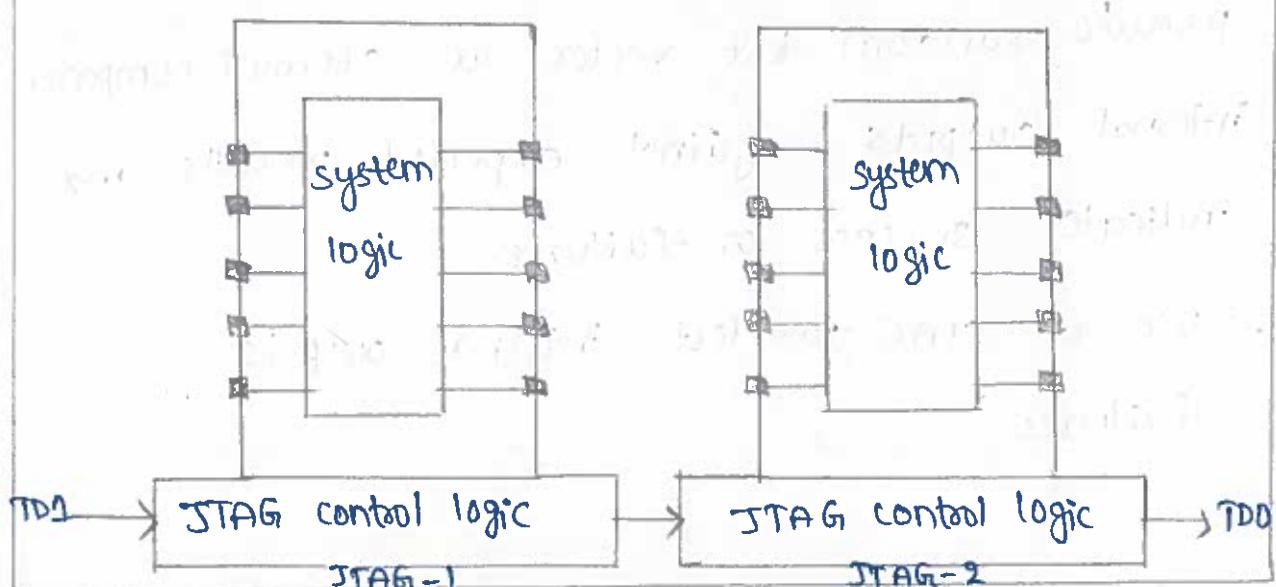


Fig: JTAG for testing internal circuitry

JTAG for external Testing:-

JTAG used for external testing of connections to other JTAG devices is shown in below fig.

Fig: JTAG for external testing of connections



→ Test Data input (TDI) is applied to first JTAG. The test data output (TDO) of first JTAG is connected to next JTAG TDI.

JTAG architecture:

JTAG architecture consists of following blocks:

- 1) Boundary scan Register (BSR)
- 2) ID code register
- 3) User definable register
- 4) Instruction register
- 5) Test Access port (TAP) controller
- 6) Instruction decoder.

→ The instruction register is serially loaded with the instruction. The operations to be performed are selected by these instructions.

→ User defined data registers are set of shift registers. The stimuli needed for an operation are loaded serially into data

registers. The results are shifted out after executing the operation.

General JTAG architecture is shown in below fig.

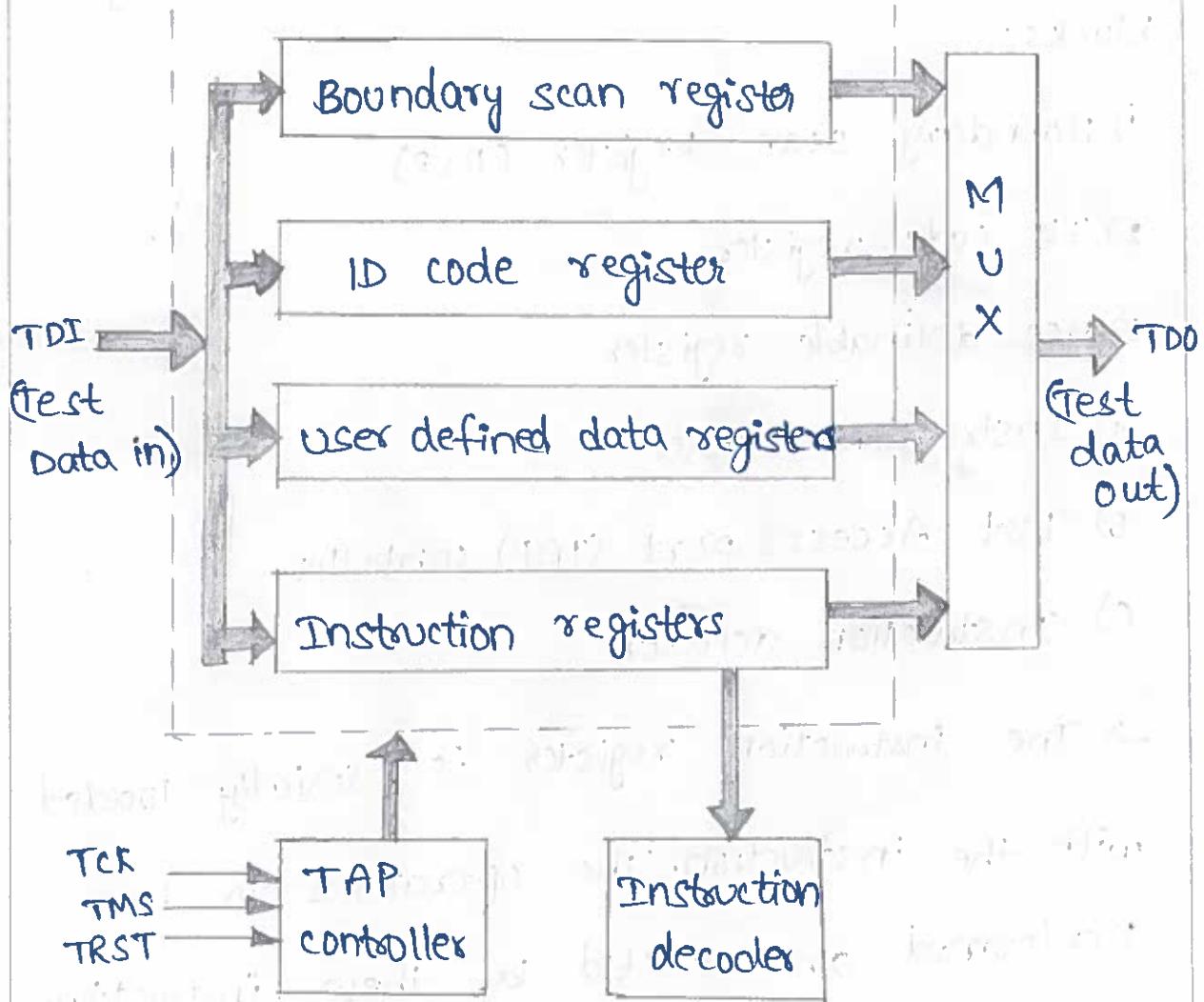


Fig: JTAG. Architecture.

→ Test Access port (TAP) is a general purpose port which provides access to control logic

for operation of JTAG. These inputs are -TCK, TMS, TRST

→ TAP controller is a finite state machine that responds to the control sequences through TAP. It generates control signals required for correcting operation.

TCK → Test clock input

TMS → Test Mode Select input

TDI → Test Data Input

TDO → Test Data output

TRST → Test Reset Input.

Built-in Self-Test (BIST):

→ With the increasing complexity of VLSI systems, test generation and application becomes an expensive and may not be an effective testing.

→ further the high speeds at which newer VLSI systems are designed to operate may not be possible to be simulated and this may create problems. These aspects can be well

handled by incorporating BIST which is mainly focused at reducing -

- a) The volume of test data
- b) costs involved in test pattern generation
- c) Test time.

→ All above points can be covered by integrating an automatic test system into the design of chip which is possible by different techniques.

These test include

- 1) Linear feedback shift Register (LFSR)
- 2) Built-in logic Block observer (BILBO)
- 3) Signature analysis.

Advantages of BIST:-

- 1) Low cost
- 2) High quality testing
- 3) Faster fault detection
- 4) Ease of diagnostics
- 5) Reduced maintenance and repair costs

- 6) Better fault coverage
- 7) capability to perform test outside the electrical testing environment.

Disadvantages of BIST:

- 1) Additional silicon area and fabrication processing requirements
- 2) Reduced access time.
- 3) Additional hardware requirements
- 4) On chip testing hardware itself can fail.

chip level and system level test:

Boundary scan check:

→ Boundary scan check is a test technique which uses scan methodology involving shift registers. The shift register control monitors signal at each input and output pins that are connected in serial fashion to form a chain of data registers called Boundary scan registers.

→ Printed circuit boards are becoming more dense and complex with use of Surface Mount Devices (SMD). Hence must test system does not guarantee good fault coverage. Boundary scan check technique involves scan path and self tests which resolves above problems.